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INTEGRATED MICROPOWER CIRCUITS

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INTEGRATED MICROPOWER CIRCUITS

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SUMMARY 10944

A study program was conducted to provide guidelines for the design of integrated micropower logic circuits. Constraints of maximum resistance, propagation time, and minimum power at frequencies below 150 kcps were imposed. Complementary Resistor-Diode-Transistor Logic offered the best trade-off performance within these constraints and state-of-the-art fabrication technology. Compatible "NAND and NOR" gates and flip-flops are feasible at frequencies ranging from 1 kcps to 150 kcps at power drains of 10 to 350 microwatts. AUTHOR

INTRODUCTION

One of the most significant advances in electronics in the past few years has been the development of microelectronic technology. Diffused silicon crystal substrates have replaced many discrete component circuits, reducing the size of electronic systems. By closely controlled processing of the integrated silicon circuits, an increase in reliability over discrete component circuits is expected.

Spacecraft electronics instrumentation will also benefit from the reduction of weight and size as well as from the increase in reliability. This appears to be obvious, but unfortunately the advantage of weight and size is slow to be fully utilized. There has been a limited implementation of microelectronics into analog functions such as receivers and transmitters and a one-for-one substitution of equivalent microelectronic functions into existing spacecraft designs will neither significantly reduce weight nor volume. Spacecraft electronic instrumentation designed within the constraint of available microelectronic functions will offer limited weight and size advantages. In most cases, those functions reducible to microelectronics do not constitute a major part of the spacecraft; therefore, it is usually more beneficial to utilize the gain in space to add more electronic capability.

There is an area where advances in microelectronics would serve to significantly reduce the weight and size of spacecraft. If the power consumed by electronic instrumentation could be reduced, this would serve to reduce battery and solar cell requirements, both significant contributors to spacecraft weight and bulk.

Microelectronic digital circuits are available in many forms of logic and are applicable to many systems employed in spacecraft telemetry and programing. However, a review of the logic forms and power consumption quickly discourages use of many of these functions except in isolated cases. The computer orientation of microelectronic logic has emphasized speed only. Little or no attention has been given to the reduction of power consumed by these circuits.

A survey of the field for low power logic showed that no thorough study had been conducted to evaluate the various logic circuits. In conventional circuitry the trend was toward complementary logic. The lack of data on micropower logic circuits and the need for micropower digital logic circuits in spacecraft stimulated the initiation of a program to evaluate the various logic schemes and to implement these circuits into state-of-the-art microelectronics. The evaluation was limited to a study of performance variations of digital circuits in typical spacecraft environment - and the application and implementation of these circuits into microelectronics by existing and proven technology. The purpose of this evaluation was to establish minimum power drain capabilities within the constraints of radiation damage, available spacecraft voltages, fan-out, fan-in, switching speed, logic levels, operating temperatures, and compatibility of the logic circuits to be developed.

The purpose of this paper is to present the results of this program and the proposed follow-on studies. Seven basic logic circuits were studied. They were Direct Coupled Transistor Logic (DCTL), Resistor-Transistor Logic (RTL), Resistor-Diode-Transistor Logic (RDTL), Emitter Coupled Transistor Logic (ECTL), Transistor-Transistor Logic (TTL), Diode-Transistor Logic (DTL), and Complementary RDTL. The detailed circuit evaluations were performed by the Sperry Semiconductor Division of the Sperry-Rand Corporation under NASA Contract NAS1 - 2179.

Employing worst-case design criteria, each of the above circuits was evaluated to determine comparative performance relative to power drain and propogation time. Next, the most promising circuits were evaluated in detail for temperature and load characteristics and finally the single most promising circuit is discussed in detail. The gate circuits are shown in figure 1. The circuit functions to be determined were NAND and NOR gates, a universal flip-flop, and applicable circuits to utilize flip-flops as shift accumulators.

The maximum resistance values were limited to 100,000 ohms to minimize the effect of radiation-induced leakage. Power-supply voltages are limited to multiples of plus or minus 1.35 volts. Performance of gates and flip-flops was to be investigated over the temperature range from minus 55° C to plus 125° C. Target values for propagation time and repetition rate were less than 1 microsecond and 150 kcps, respectively.

PRELIMINARY CIRCUIT EVALUATION - COMPARATIVE PERFORMANCE

For each configuration investigated, five gates were built and connected in a closed loop to form a ring oscillator. Power drain and propagation time per stage for the ring oscillator are used as performance criteria. The curves in figure 2 are a summary of the results of this test for each configuration. Component values for the gates were

optimized by use of the worst-case design equations. Basic circuits are shown in figure 1.

It is not readily apparent from the curves in figure 2 which of the circuit configurations is better. RTL, DCTL, and RDTL are easily eliminated. The excessive power drain of RTL is sufficient for elimination. DCTL is subject to current "hogging" and RDTL must be operated at low voltages to obtain the curve in figure 2. Operation of RDTL at low voltages makes it sensitive to resistor and transistor beta variations. Although TTL appears to be optimum, the requirements of low inverse beta to prevent current hogging must be studied in detail. ECTL shows no improvement in performance over DTL and is more complex both in the gate and flip-flop configuration. Therefore, DTL will be studied in detail. CRDTL appears attractive by virtue of the ease by which NAND and NOR gates may be designed. In addition, significant power reduction is achieved without drastic reduction in supply voltages. Beta requirements per fan-out must be studied as they appeared to be excessive.

The results of the preliminary study eliminated all but TTL, DTL, and CRDTL. A tabulated review of test parameters is shown in tables 1 and 2. In order to ascertain the optimum circuit with the constraint outlined in the introduction, a detailed study of the gating and flip-flop functions over temperature and frequency is necessary. The evaluation of TTL, DTL, and CRDTL digital circuits was based on the derivation of minimum power drain gates, flip-flops, and power drivers. The flip-flops should have a d-c set or reset and a-c sets and resets. NAND and NOR gates must be designed. In addition to the constraints outlined at the beginning of this paper, beta requirements per fan-out were studied. Final selection of the digital circuit was based on performance variation studies as a function of component variations and loading characteristics at constant power drain - and propagation time as a function of variable power drain.

CIRCUIT PERFORMANCE VARIATONS

The three circuits, DTL, TTL, and CRDTL, selected for detailed evaluation were designed to employ the same transistors. Transistors with three ranges of beta were used consistently throughout this phase of the study. Performance variations of gates and flip-flops under load and over temperature excursions are of prime interest. Each of the logic circuits under study was used to form NAND and NOR gates and flip-flops where possible.

Complementary Resistance Diode Logic (CRDTL)

Complementary RDTL gates as shown in figure 1 were not designed to be truly complementary. If applied voltages are to be kept below 3 or 4 volts, the design of an exact complementary gate with design criteria to provide equal base currents and turn-off voltages is not feasible. This is due to the conflicting beta requirements for the transistors and variations in transistor turn-off voltages. R_1 in figure 1(f) was varied to achieve nearly equal base currents and turn-off voltages which yielded nearly equal transistor beta requirements per fan-out. The compromise complementary circuits are shown in figure 5 with tabulated values of circuit parameters. Resistor tolerances were varied from plus or minus 10 percent to plus or minus 5 percent for this design to determine the effect of changing this design criteria on circuit performance. It was felt that an investigation of the performance characteristic of one or two designs would offer greater insight into performance limitation not immediately apparent. The circuit parameters shown in figure 5 were chosen for a typical design. The power drain of this gate is approximately 500 microwatts. Lower power drain gates can be achieved with increased resistances but there would be a subsequent decrease in switching speed. For the gate tests a group of limit samples was selected to determine the effect of transistor storage time, frequency response, and beta on circuit performance.

Figures 6 and 7 show rise and fall times for "speedup" capacitance values of 15 and 50 μμf for complementary NAND and NOR gates. Variations of performance due to transistor beta, storage time, and loading conditions are also shown. Worst-case conditions are shown in figure 8 with speedup capacitance values of 50 and 75 μμf.

The CRDTL flip-flops were designed around the circuit in figure 9. It is a standard configuration utilizing speedup capacitance and conventional steering. The values that permitted the best power drain, repetition rate, and loading characteristic with gates are also shown. Worst-case operating characteristics over temperature are shown in figure 10 for pulse and square wave operation. Optimum performance over temperature was obtained with values of 50 μμf for C_1 and 75 μμf for C_2. Power drain is approximately 250 microwatts.

Diode-Transistor Logic

The gate configuration shown in figure 1(e) exhibited the most preferable trade-off between beta requirements, noise margin, propagation time, and power drain for DTL. The design selected for evaluation of performance variations is shown in figure 11. Transistors were employed with a combination of maximum and minimum betas with maximum and minimum storage times. The effect of the switching speed of the two coupling diodes is also considered. The table in figure 11 is a result of tests of various diodes in the DTL configuration. Propagation time versus temperature measurements were made for combinations of transistors and coupling diodes. Figure 12 shows the propagation time for the 300-nanosecond recovery time diodes.

The DTL flip-flops are essentially two cross-coupled DTL gates with associated steering networks. Two circuits considered are shown in figure 13. Collector supply voltage levels of 2.7 volts were used throughout. Design values for figure 13(a) are also shown; however, they were not optimized. Performance of the flip-flop as a function of temperature and transistor variations is shown in figure 14. The flip-flop in figure 13(b) was also evaluated and resulted in higher operating frequency. However, the noise margin prohibits further consideration as discussed earlier unless operating frequency is of paramount importance. The lowest power drain for the flip-flop is 580 microwatts.

Transistor-Transistor Logic (TTL)

The TTL configuration under test is shown in figure 1(c). The most significant problem with TTL is the relationship of inverse beta and base bleed-off current. The TTL configuration seemed to have

TABLE 1.- SUMMARY OF LOGIC CIRCUIT TEST RESULTS

Circuit	Circuit type	Propagation time / Stage	Power drain	Maximum noise immunity	Beta/N	Fan-in	Maximum R
T^2L	Direct coupled	0.5 μsec	110 μW	200 mv	3.5 at N = 5	3	50K
DCTL		.5 μsec	320 μW	250 mv	7.5 at N = 3	3	45K
		.5 μsec	360 μW	250 mv	6.5 at N = 5	3	30K
ECTL		.5 μsec	200 μW	100 mv	2.0 at N = 5	3	48K
		.5 μsec	240 μW	700 mv	5.5 at N = 5	3	36K
CRDTL	Complementary	.5 μsec	260 μW	350 mv	9.0	3	75K
RDTL	Single transistor gate	.5 μsec	420 μW	500 mv	11.0	4	75K
DTL		.5 μsec	105 μW	200 mv	4.0	3	180K
		.5 μsec	310 μW	400 mv	6.0	3	75K
		.5 μsec	190 μW	600 mv	5.0	3	100K

TABLE 2.- SUMMARY OF LOGIC CIRCUIT TEST RESULTS

Circuit	Circuit type	Propagation time / Stage	Power drain	Maximum noise immunity	Beta/N	Fan-in	Maximum R
T^2L	Direct coupled	0.5 μsec	110 μW	200 mv	3.5 at N = 5	3	50K
CDGTL		.6 μsec	220 μW	250 mv	7.5 at N = 3	3	50K
		.88 μsec	216 μW	250 mv	6.5 at N = 5	3	50K
ECTL		.56 μsec	178 μW	100 mv	2.0 at N = 5	3	50K
		.58 μsec	210 μW	700 mv	5.5 at N = 5	3	50K
RTL (modified)		1.22 μsec	95 μW	200 mv	4.0 at N = 6	3	50K
CRDTL	Complementary	.35 μsec	450 μW	350 mv	10.0	3	50K
		.25 μsec	250 μW	150 mv	12.0	3	50K
RDTL	Single transistor gate	.17 μsec	1000 μW	500 mv	11.0	4	50K
DTL		.18 μsec	385 μW	200 mv	4.0	3	50K
		.4 μsec	405 μW	400 mv	6.0	3	50K
		.3 μsec	395 μW	600 mv	5.0	3	50K

conflicting requirements of forward and inverse beta. Three groups of gate transistors were selected with ranges of inverse beta of 0.5 to 0.7, 0.2 to 0.3, and 0.1 to 0.15, and ranges of forward beta of 75 to 100, 20 to 40, and 10 to 20, respectively, and are referred to as high-, medium-, and low-range transistors. Minimum turn-off voltages for ranges of fan-out and fan-in are shown in figure 15. Figure 16 shows percentage of maximum base current variations as a function of gate fan-in and fan-out for each of the inverse beta ranges investigated. In figure 17 is shown rise and fall time propagation time relationship versus temperature for conditions where the rise and fall times above have been optimized for propagation time with beta and storage time variations.

Since the TTL flip-flop is a direct-coupled circuit, the output voltage is quite small. It is also quite complex. It may be analyzed by utilizing TTL gate data. Frequency of operation was in excess of 100 kc. However, the power drain and complexity ruled out TTL flip-flops.

CONCLUSION

The circuits and parameters are not necessarily the design recommended. The intention of this study was to evaluate performance variations as a function of power drain, component variation, and loading. The evaluation then permits selection of an optimum logic circuit design with the constraints outlined at the beginning of this paper.

From the data, TTL permits the lowest power drain and exhibited consistent performance over temperature. However, low inverse beta requirements and low turn-off voltages for the gates severely affect base current variations and noise immunity. There are conflicting requirements of low inverse beta to prevent base current reduction and high forward beta to provide low offset voltages to minimize the turn-off voltage problem. In addition, rigid component selection and the complexity of the flip-flop constitute serious drawbacks. The TTL flip-flop requires the equivalent of eight gates and the power drain is subsequently quite high and prohibits the use of a-c steering networks due to the direct coupling required.

Diode-transistor logic and complementary resistance-diode-transistor logic (RDTL) permit a-c coupling. DTL consistently showed poor performance at low voltages and over temperature excursions. In addition, NAND and NOR gates are not directly available in the basic DTL configuration. Flip-flops employing a-c steering are available and may be adapted to a shift accumulator, but the performance over temperature is poor.

Complementary RDTL does permit NAND and NOR functions to be easily fabricated with similar design and performance characteristics. The versatility of the complementary gate allows greater flexibility in design. This includes a readily available inverted pulse to drive additional NAND and NOR gates. Transistors switching on for each logic level in complementary RDTL allows speedup of fall times, enhancing switching speeds. The worst-case propagation time degrades at high temperature, but not as badly as DTL. Noise immunity is better than TTL. Fan-out requirements impose a high beta requirement on complementary pair transistors, but it is not prohibitive.

The complementary flip-flop is less complex than two gates and has considerably less power drain than the other flip-flops considered. Finally, a-c set and reset are possible and shift accumulator features are readily available. Therefore, within the constraints outlined earlier in this paper, complementary RDTL logic appears to offer the best performance characteristics. As operating frequencies are increased above 200 kcps, DTL appears to offer better performance trade-offs. At frequencies in excess of 1 megacycle per second, DTL probably offers the best performance characteristic.

The implementation of these circuits into usable microelectronic hardware must be considered. The requirements of complementary NPN/PNP high beta, low-current transistors is not consistent with the state of the art in single-chip integrated circuits. Complementary transistors with high betas at low currents are difficult to fabricate but they are available. The only constraints imposed upon packaging were the maximum number of semiconductor chips which may be utilized to fabricate the individual logic circuits and the packaging configuration.

The complementary gates and flip-flops will be constructed by proven technology. Separate chips of semiconductor integrated components will be employed and interconnection will be thermocompression banded gold wires. The state of the art prohibits a single-chip approach. Beta control of NPN silicon planar transistors during fabrication is relatively easy while PNP is not. As the beta is increased, control during doping becomes more difficult and again the PNP transistor suffers more than the NPN. This becomes even more difficult with transistors of high beta at low current. Fabrication of single-chip PNP/NPN planar complementary devices involves problems of selective epitaxy, precise emitter diffusion control, and selective cleaning processes which are different for NPN and PNP surfaces. Today no solution exists for these problems. It is felt that NPN/PNP complementary high-beta, low-current devices can best be fabricated by isolation diffusion techniques. These techniques are not yet amenable to integrated circuit designs with stringent requirements for low C_b and stray capacitance. The parasitics in isolation diffusion technology also contribute to undesired power drain. For these reasons, it was felt that a multi-integrated chip approach would be the most expedient.

Final specifications have not been determined, but initial guidelines for flip-flop and gate fabrication have been formed. The NAND and NOR gates will be fabricated employing a maximum of three chips per gate. The flip-flops will utilize a maximum of six chips.

This is only the first step to ultimate integration of complementary RDTL into single-chip integrated circuits.

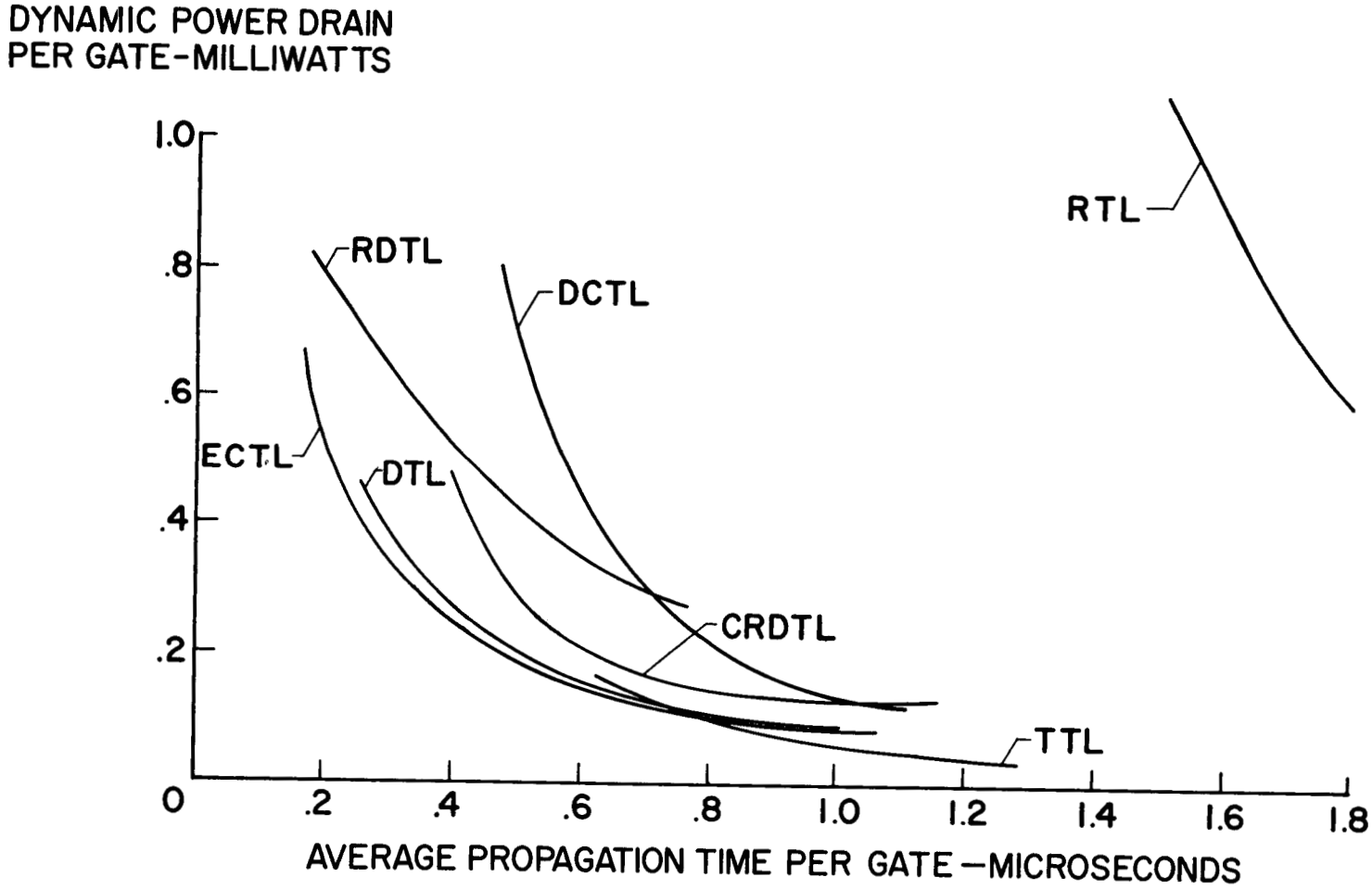

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Figure 2.- Power drain versus propagation time for various logic gate circuits.

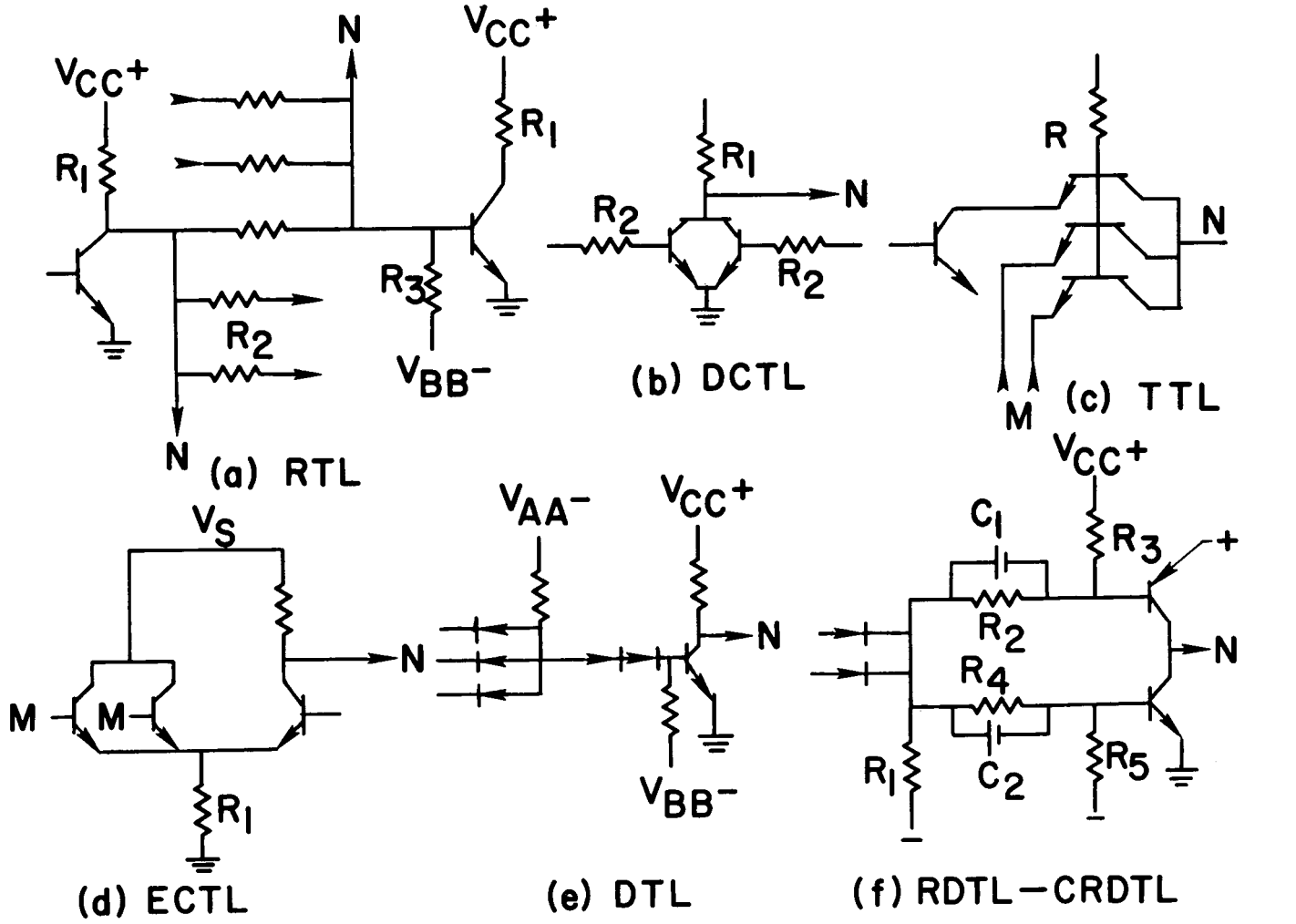

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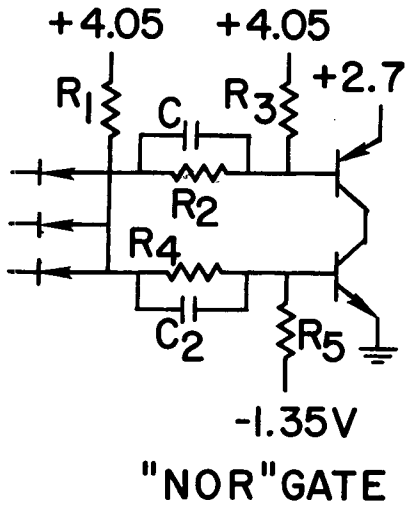
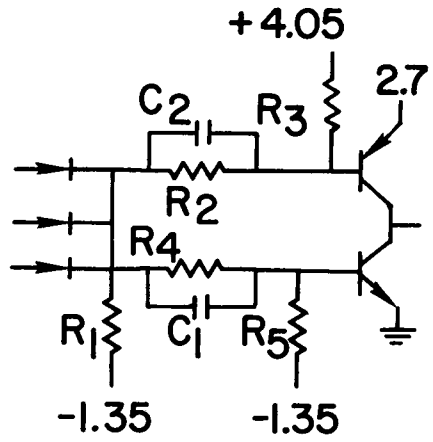
Figure 1.- Basic diagrams of logic circuits evaluated.



"NOR" GATE



"NAND" GATE

						IB(μa)		VBE OFF		B_f IN	
R_1	R_2	R_4	R_3	R_5	R(TOL)	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
45,000Ω	20,000Ω		50,000Ω		5%	21	26.6	.19	.185	6.7	5.3
					7.5%	18.3	23.8	.24	.205	8.0	6.2
					10.0%	15.7	21.0	.29	.234	9.6	7.2

FOR C_1 AND C_2 VALUES SEE FIGURES 6,7 AND 8

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Figure 3.- NAND-NOR logic circuits CRDTL and parameters.

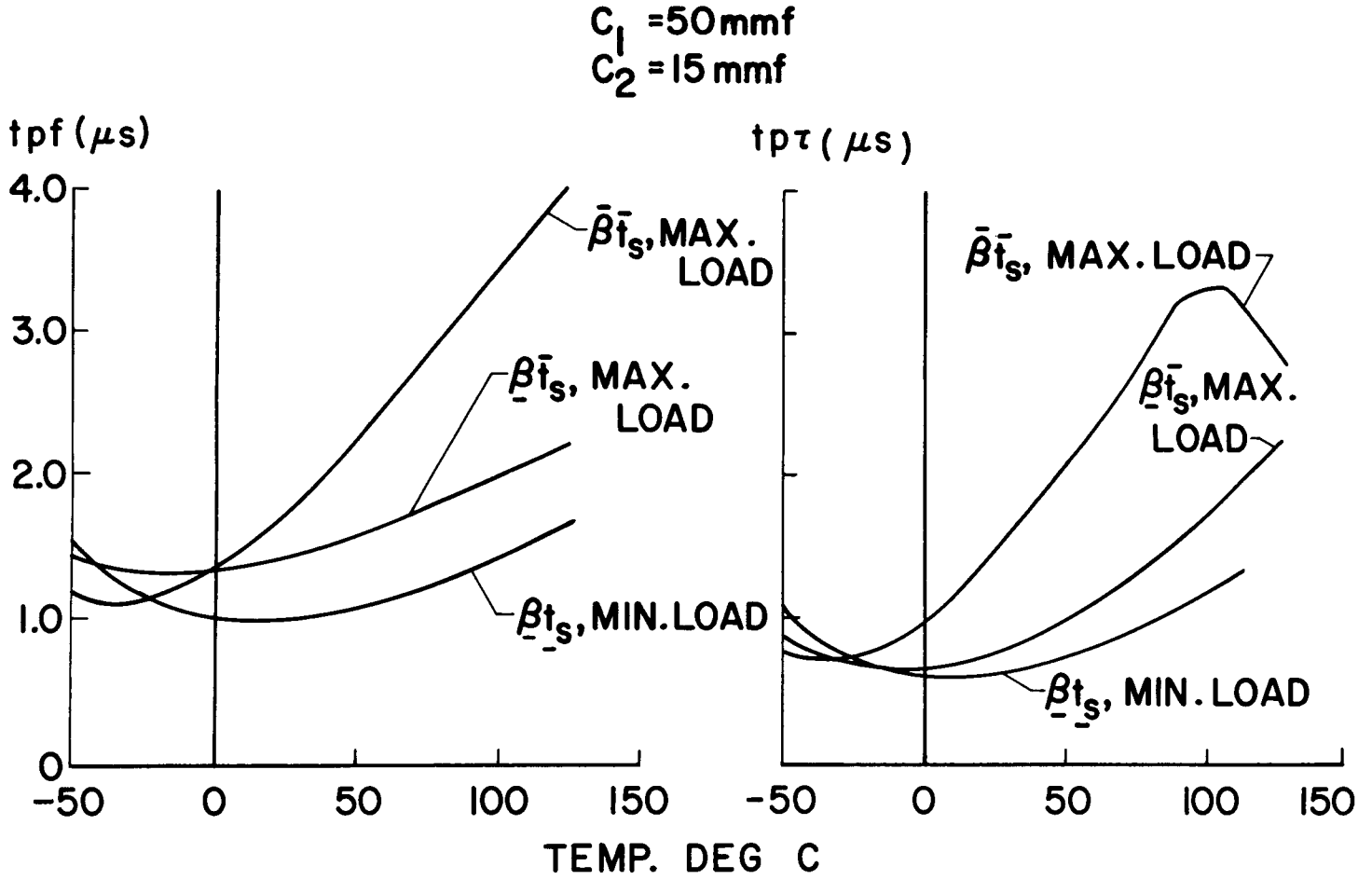

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Figure 4.- Complementary RDTL-NAND gate propagation time versus temperature.

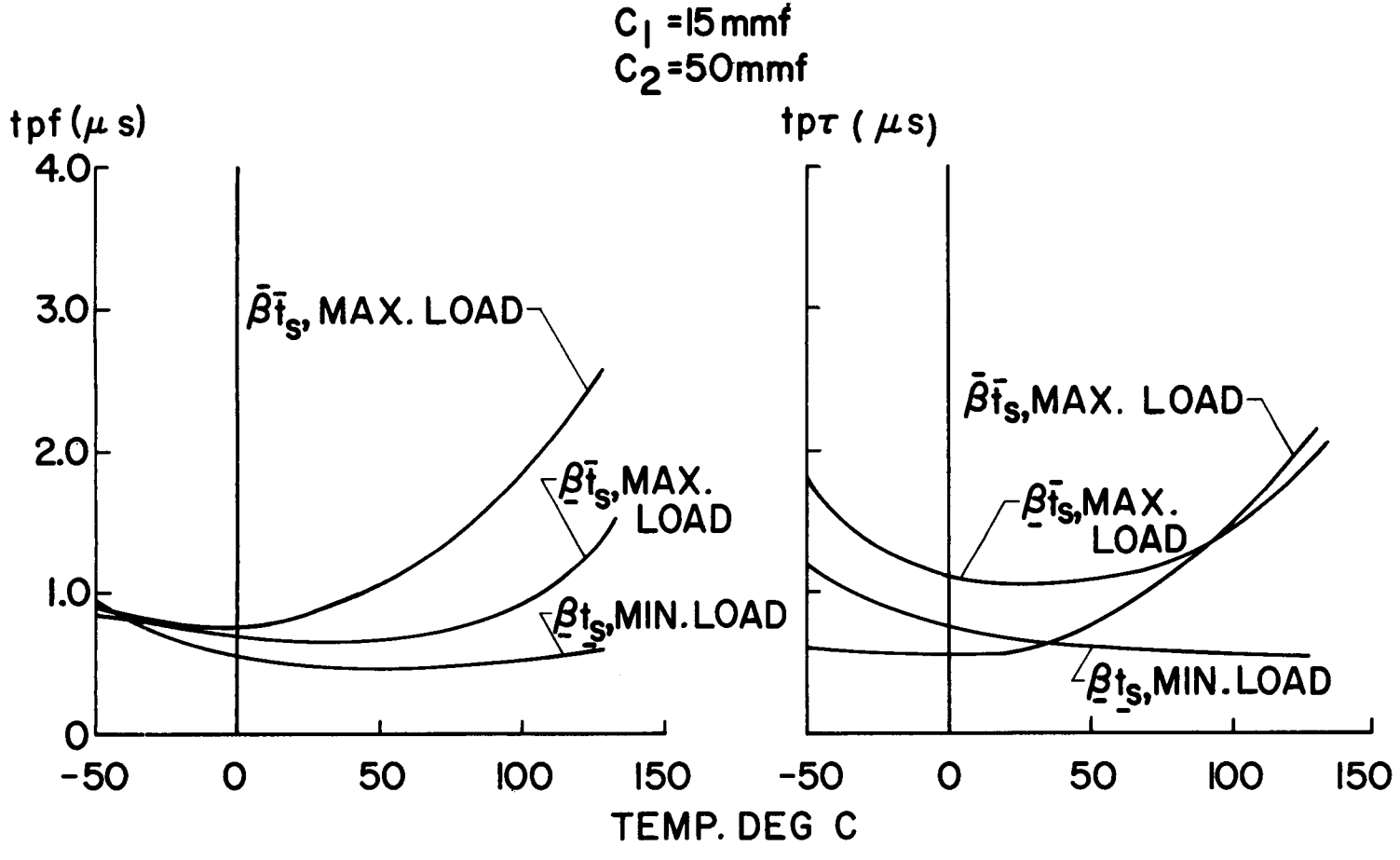

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Figure 5.- Complementary RDTL-NOR gate propagation time versus temperature.

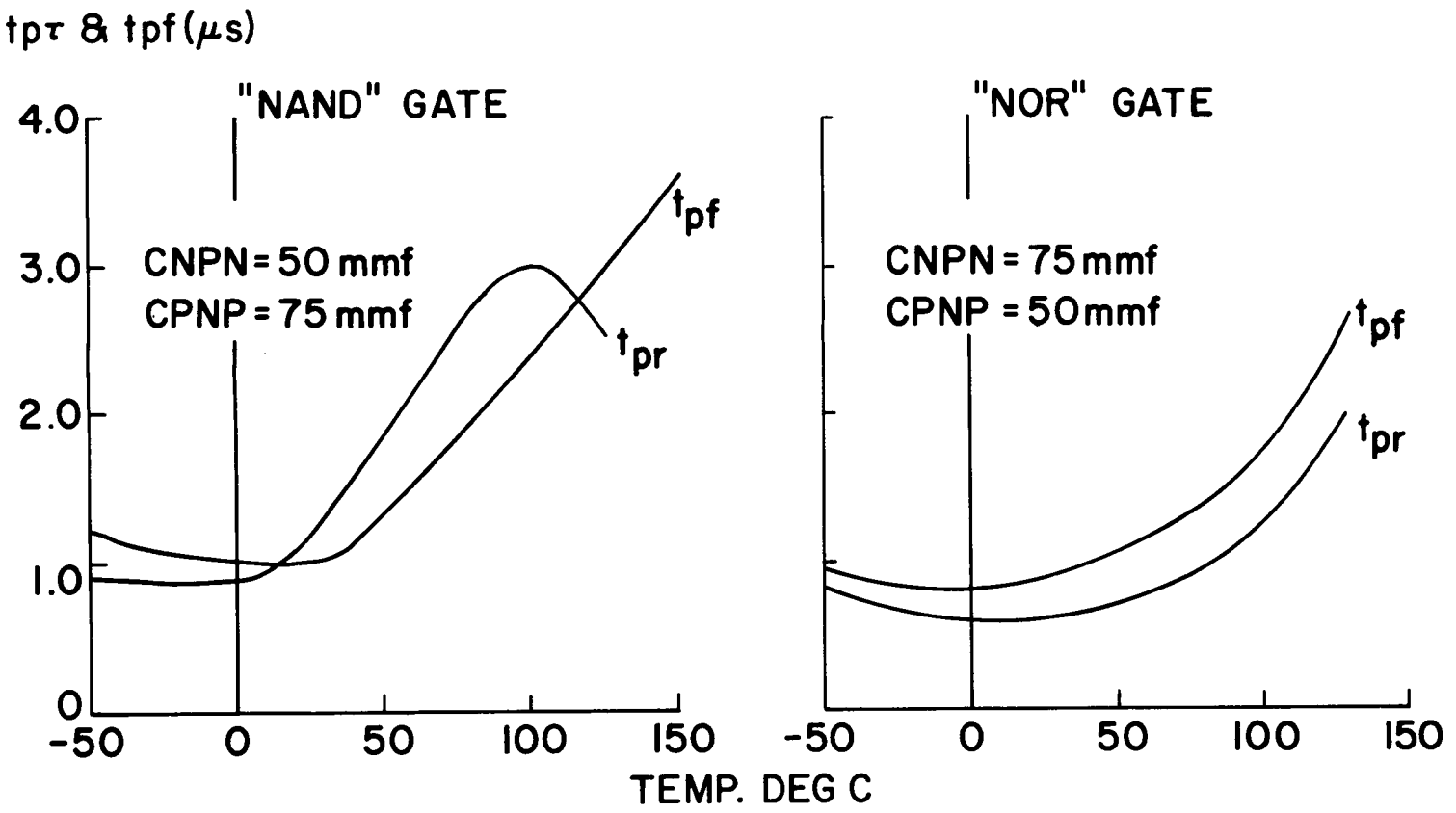
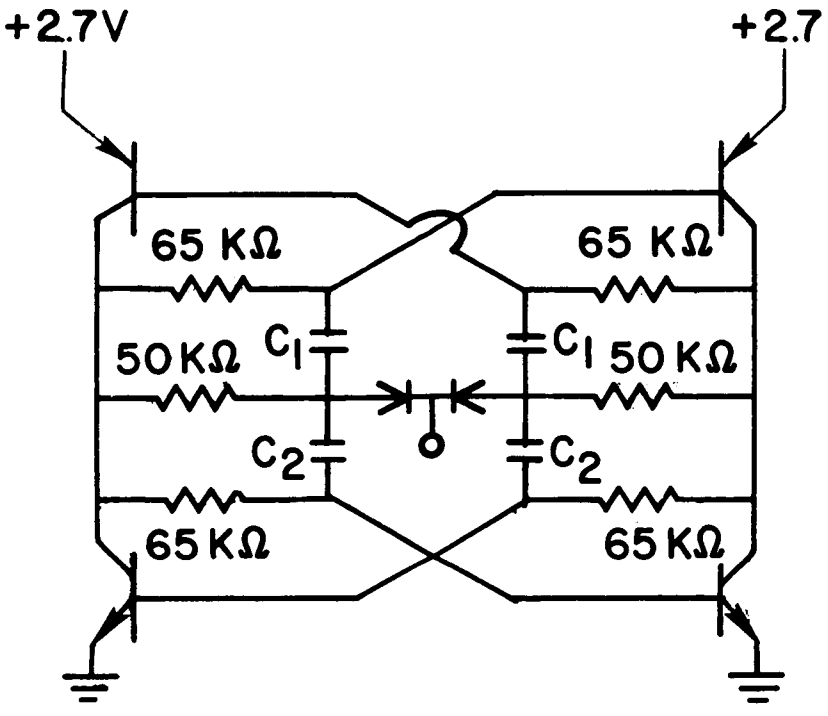


Figure 6.- Worst case complementary RDTL gate design β maximum t_s maximum $t_{p\tau}$ and t_{pf} versus temperature.



C_1 = 50 mmf AND C_2 = 75 mmf

POWER DRAIN = 250 μ WATTS

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Figure 7.- CRDTL flip-flop design.

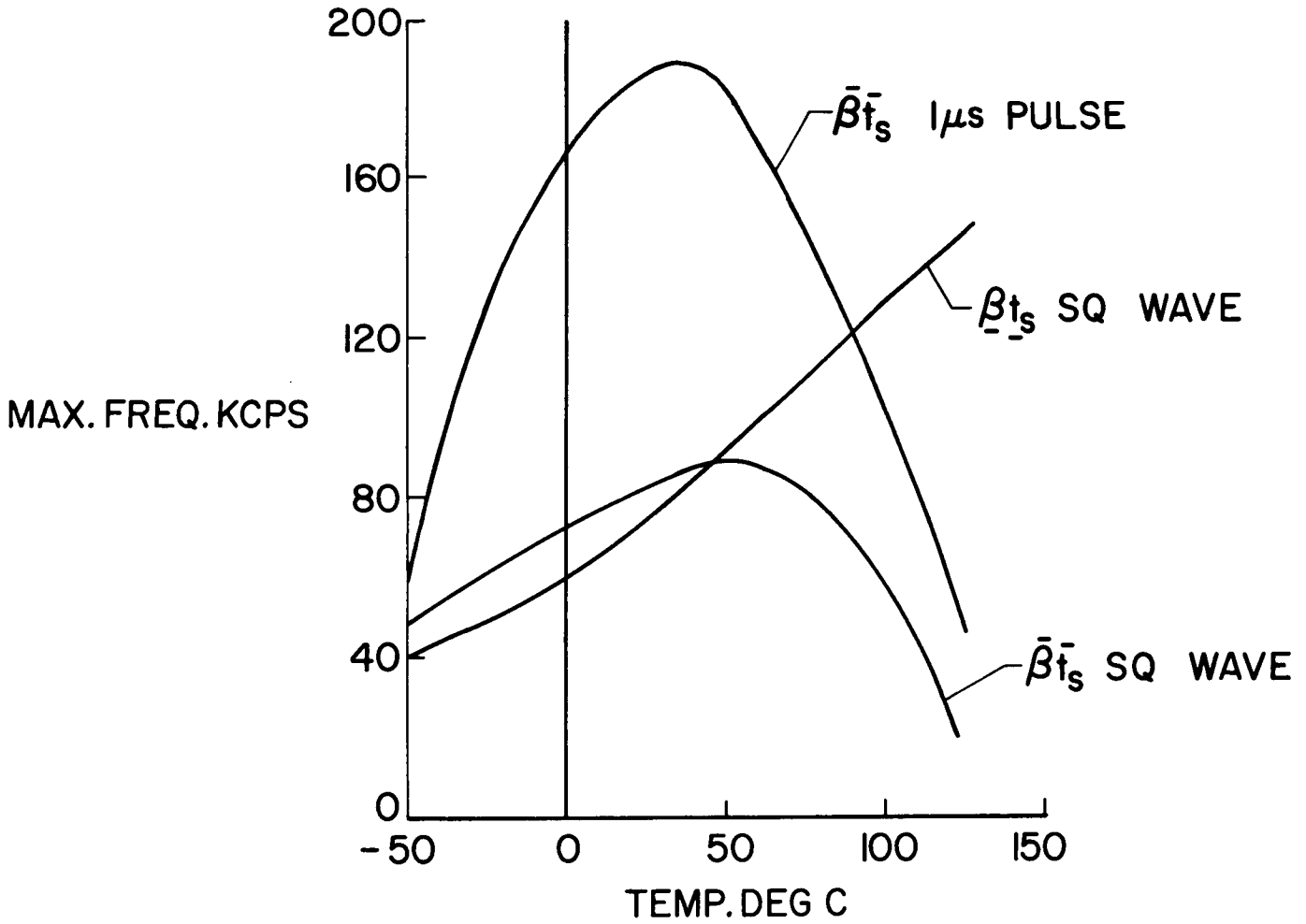

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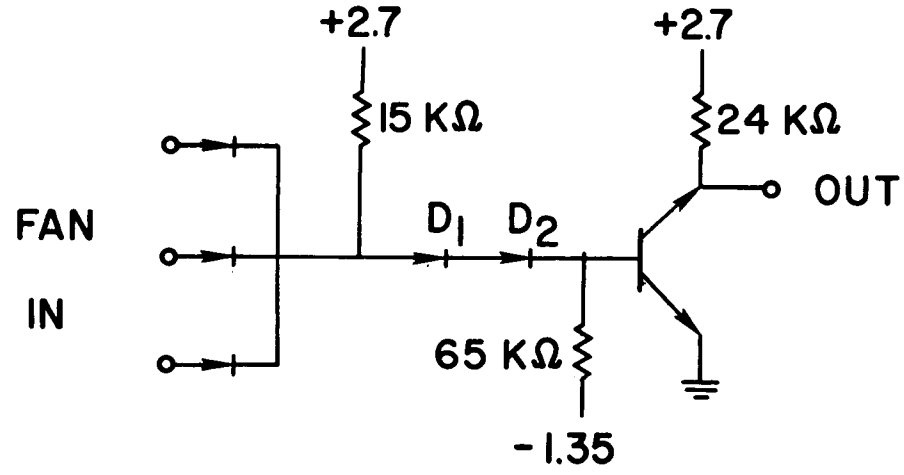
Figure 8.- Complimentary RDTL flip-flop maximum operating frequency versus temperature.



REVERSE RECOVERY TIME TO 0 VOLTS AT I_f = 5 ma MICRO SECONDS	T_{pr} MICROSECONDS	T_{pf} MICROSECONDS
.03	1.7	1.66
:06	1.5	1.77
.1	1.2	1.08
.3	.9	1.0
.7	.6	.84

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Figure 9.- DTL gate circuit.

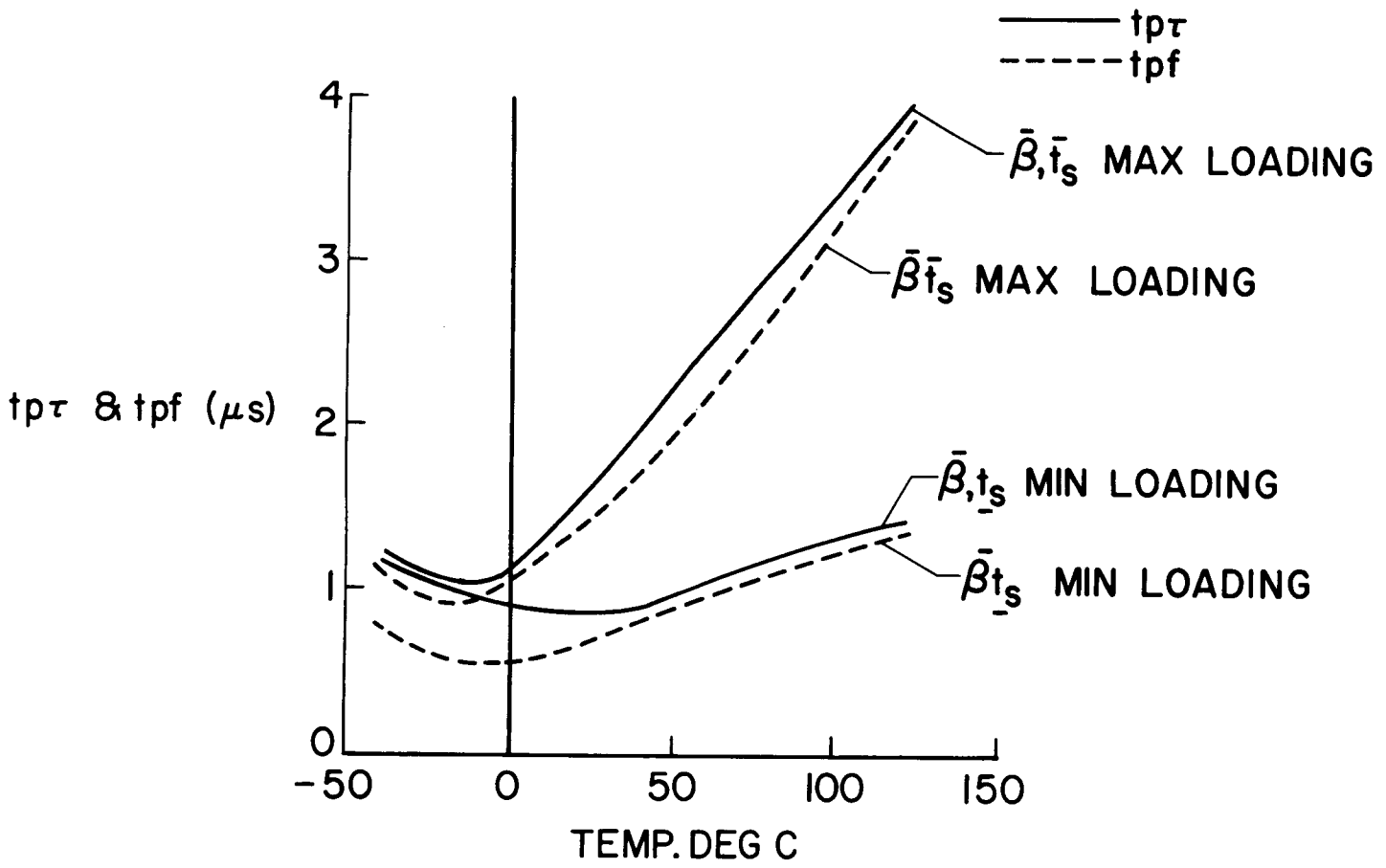

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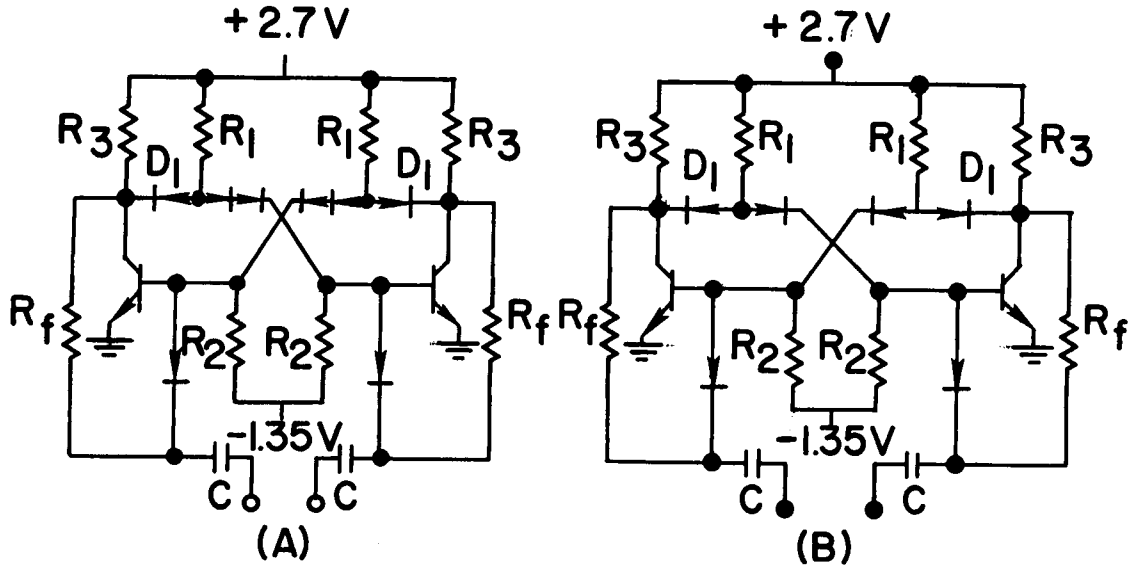
Figure 10.- DTL gate propagation time of rise and fall times versus temperature.



R_1 KΩ	R_2 KΩ	R_3 KΩ	R_f KΩ	POWER DRAIN μ WATTS	OPERATING FREQ KCPS		
					C=100mmf	C=75mmf	C=68mmf
12	50	22	20	1150	140	125	95
15	62	24	27	925	140	130	125
18	80	33	33	725	100	100	95
24	100	39	43	580	100	100	90

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Figure 11.- DTL flip-flop test circuits.

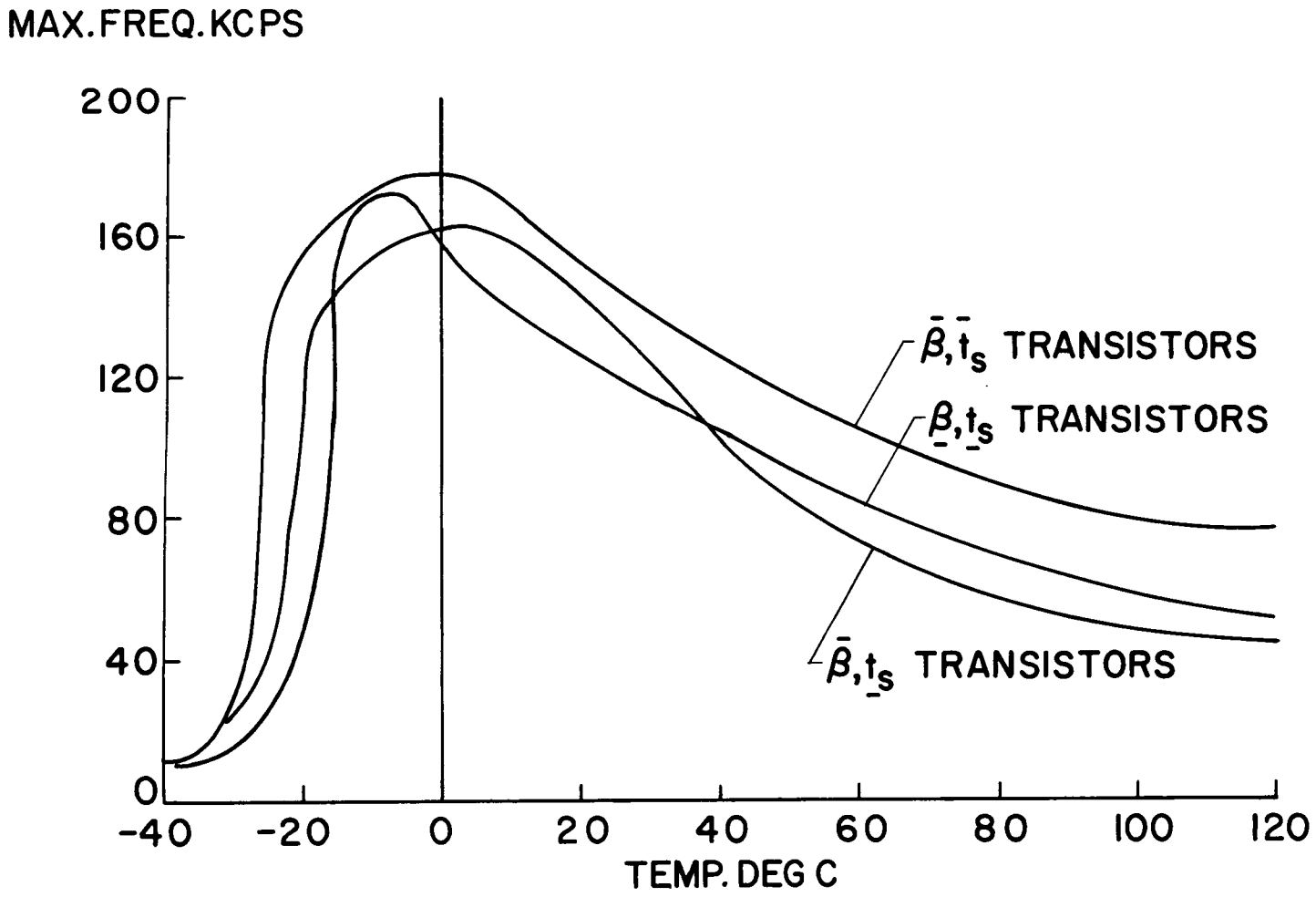

Figure 12.- DTL flip-flop maximum frequency versus temperature - 50-percent duty cycle.

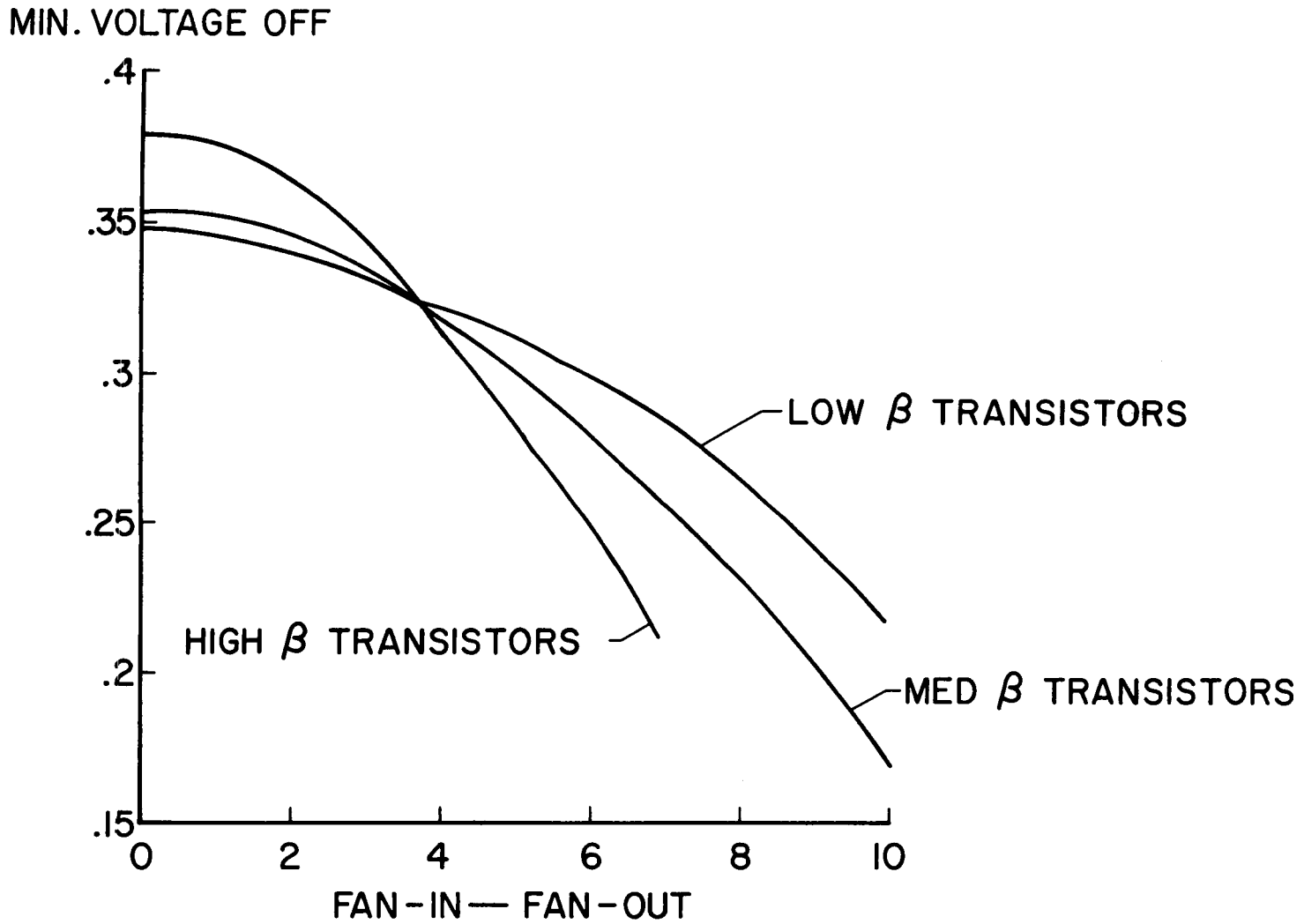

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Figure 13.- TTL gates voltage off versus fan-in and fan-out.

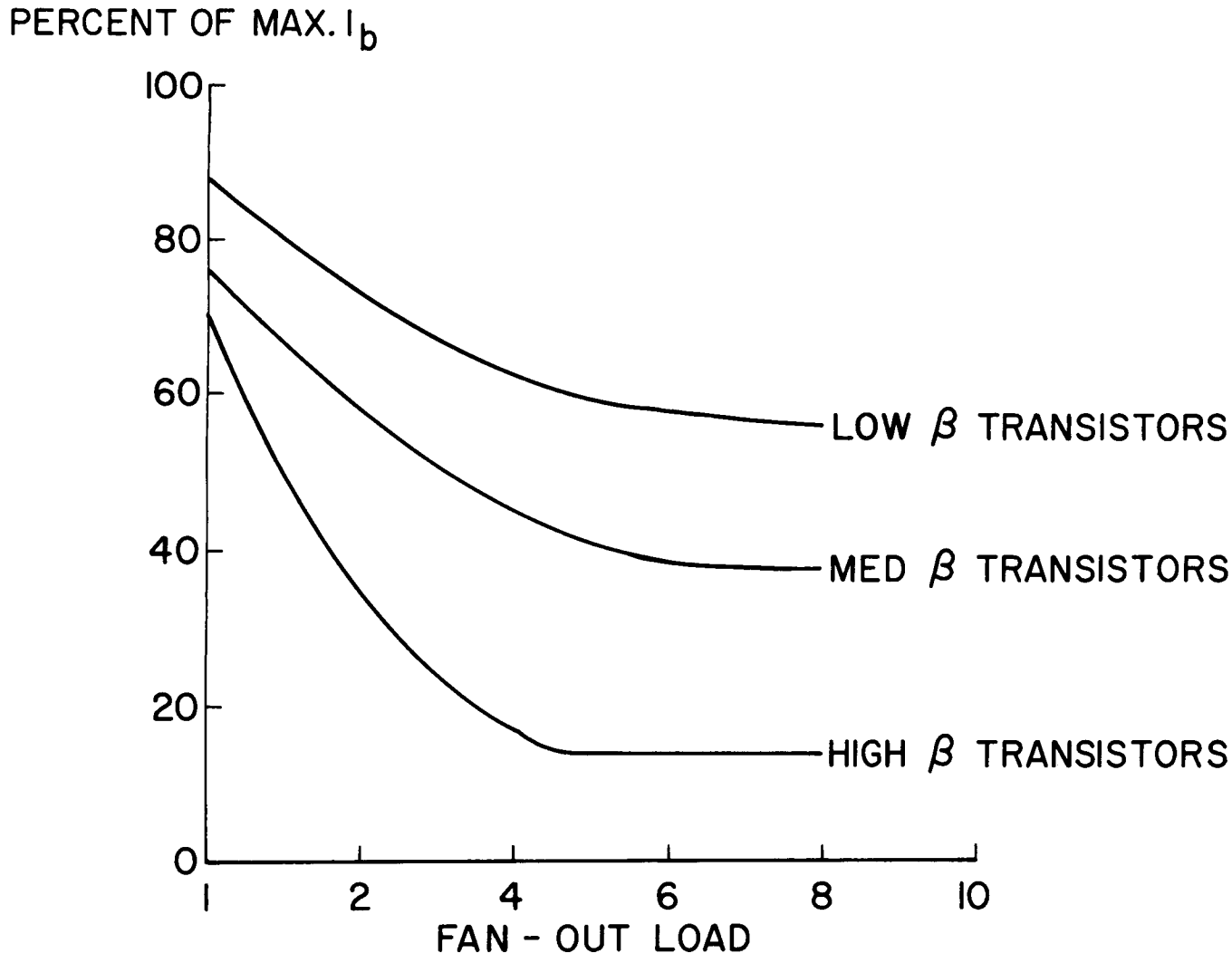

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Figure 14.- TTL gates I_b variation fan-in of four versus fan-out.

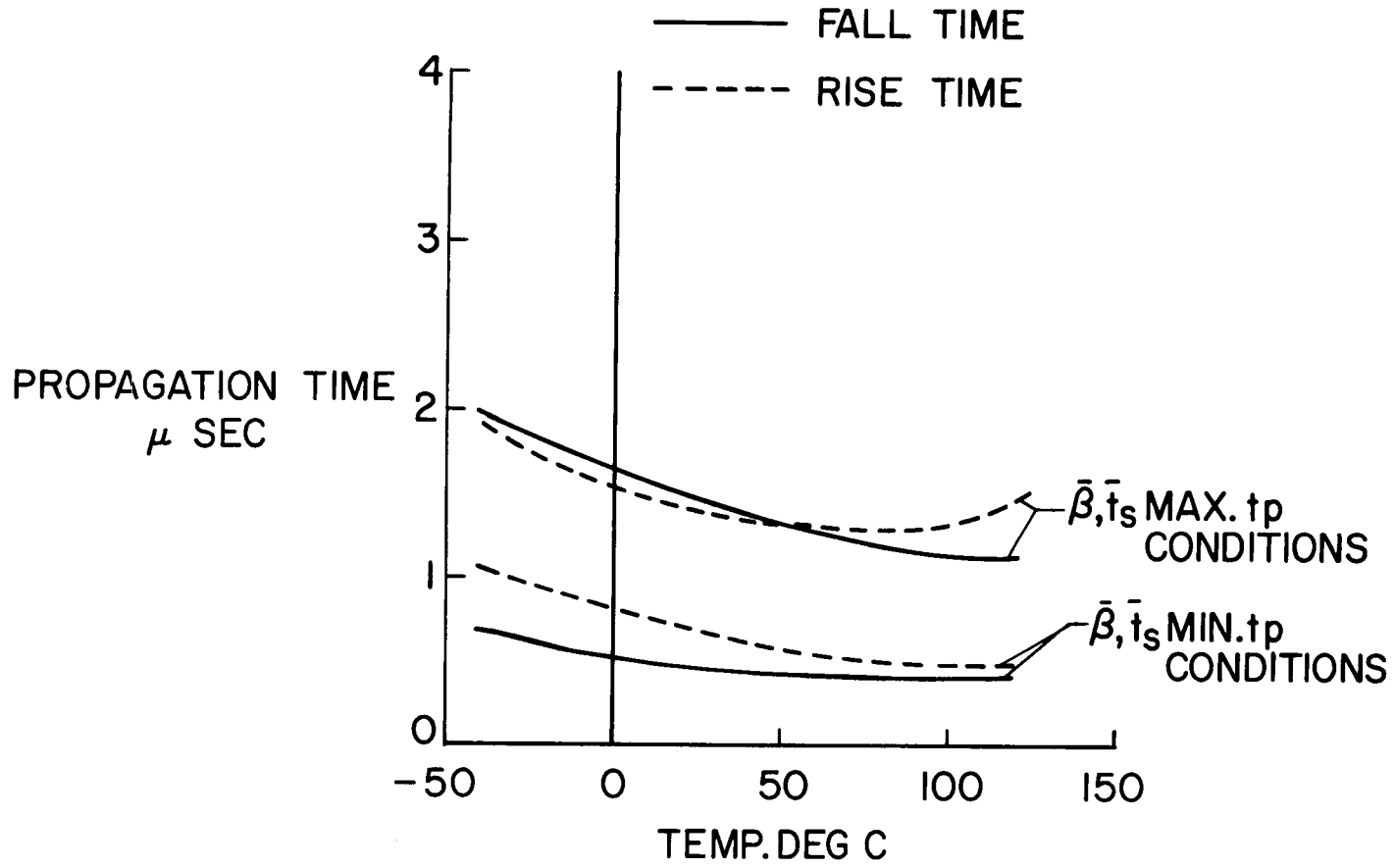

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Figure 15.- TTL gate propagation time versus temperature.